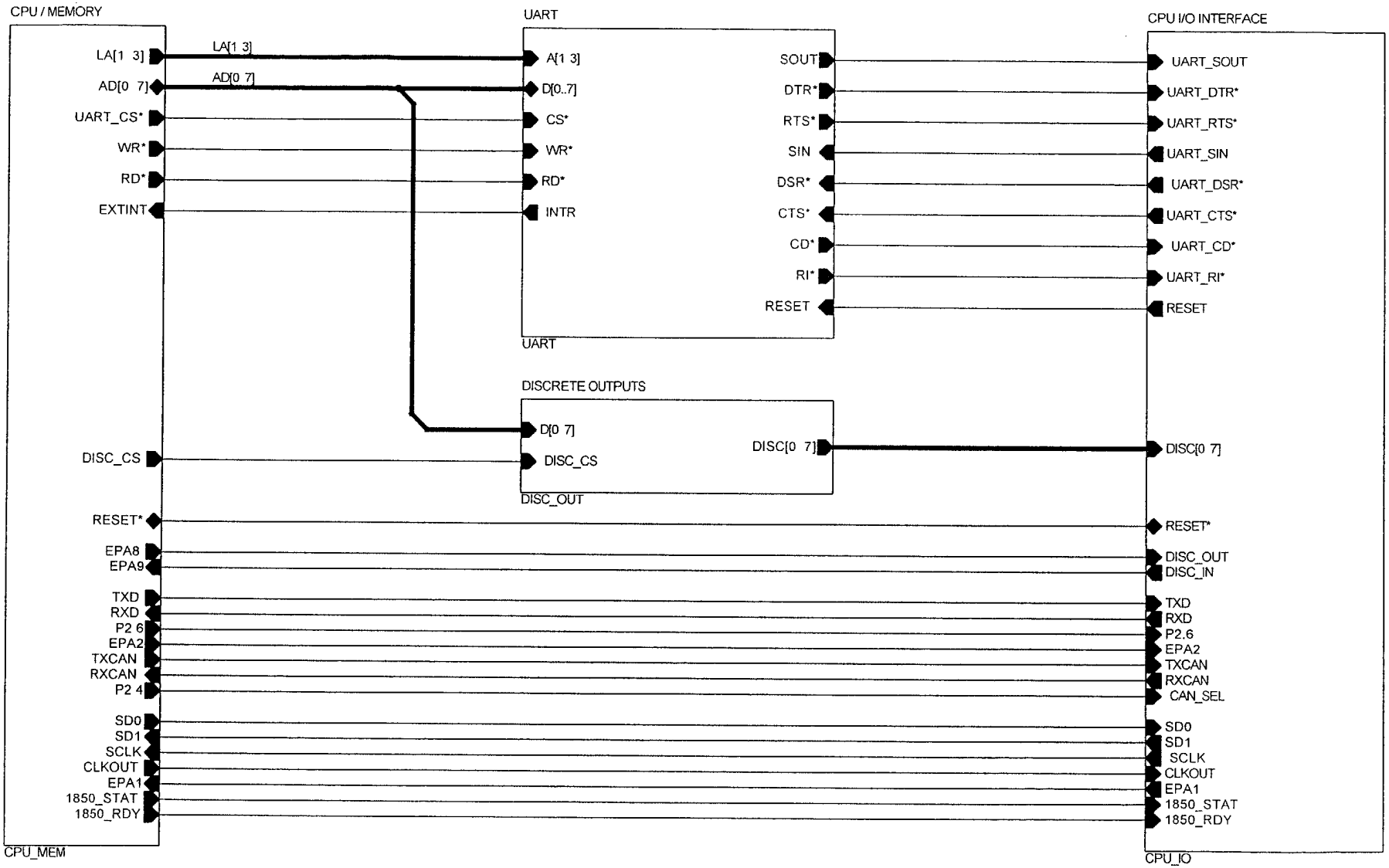



FIG 1

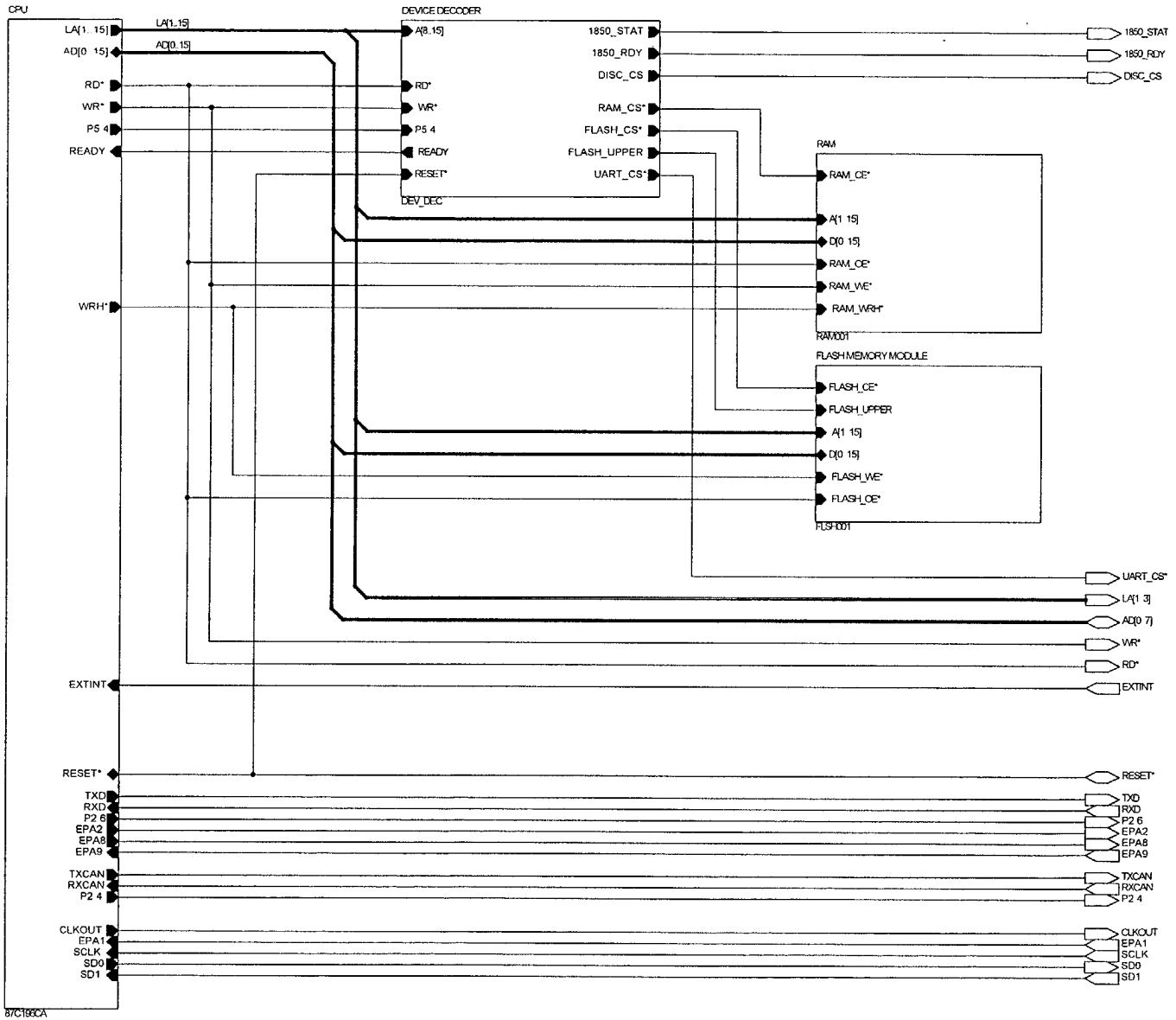

CPU
LA[1..15]
AD[0..15]
RD*
WR*
P5.4
READY
WRH*
EXTINT
RESET*
TXD
RXD
P2.6
EPA2
EPA8
EPA9
TXCAN
RXCAN
P2.4
CLKOUT
EPA1
SCLK
SD0
SD1
87C196CA
DEVICE DECODER
A[8..15]
RD*
WR*
P5.4
READY
RESET*
1850_STAT
1850_RDY
DISC_CS
RAM_CS*
FLASH_CS*
FLASH_UPPER
UART_CS*
DEV_DEC
RAM
RAM_CE*
A[1..15]
D[0..15]
RAM_CE*
RAM_WE*
RAM_WRH*
RAM001
FLASH MEMORY MODULE
FLASH_CE*
FLASH_UPPER
A[1..15]
D[0..15]
FLASH_WE*
FLASH_OE*
FLSH001
1850_STAT
1850_RDY
DISC_CS
UART_CS*
LA[1..3]
AD[0..7]
WR*
RD*
EXTINT
RESET*
TXD
RXD
P2.6
EPA2
EPA8
EPA9
TXCAN
RXCAN
P2.4
CLKOUT
EPA1
SCLK
SD0
SD1

FIG 2

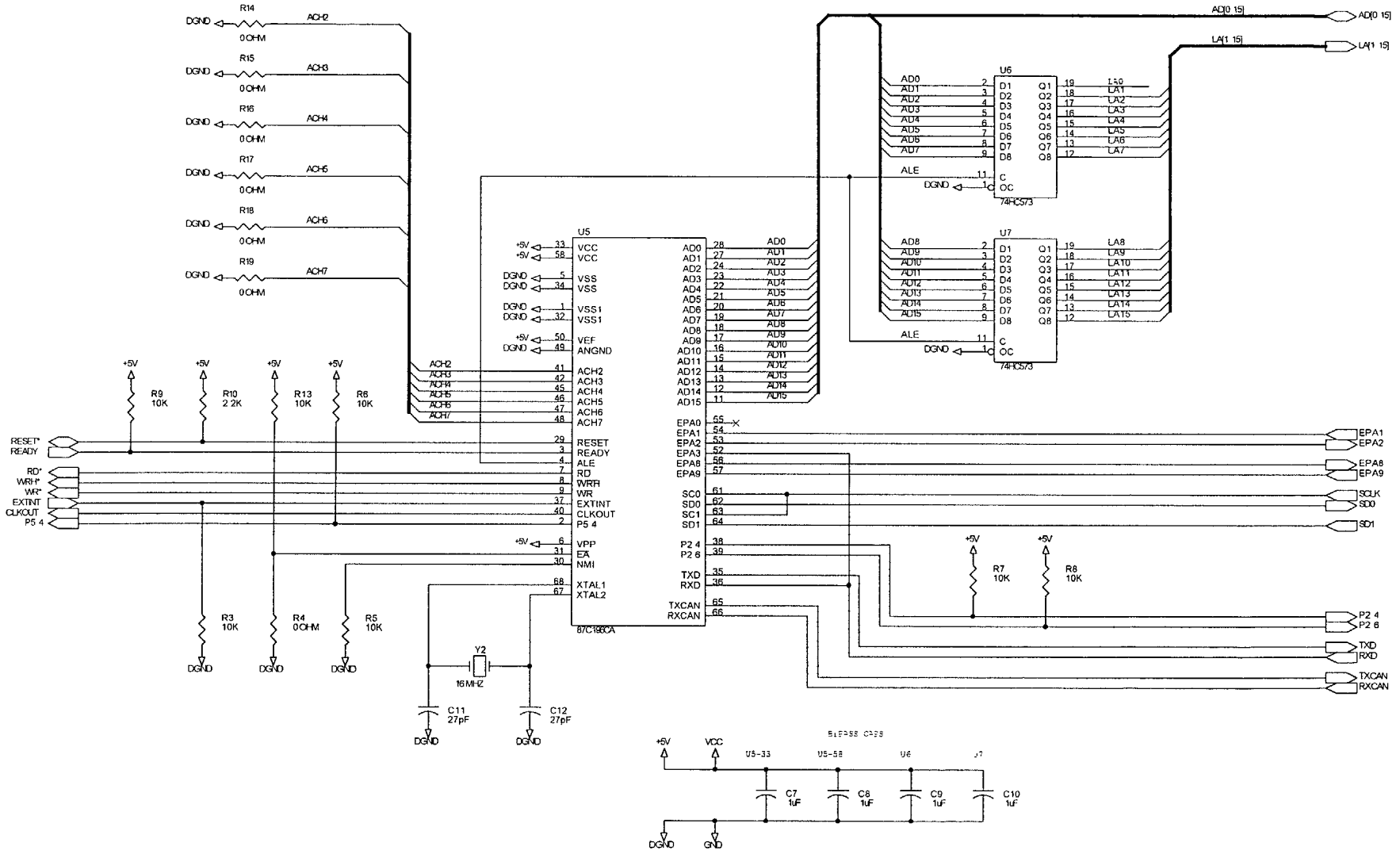
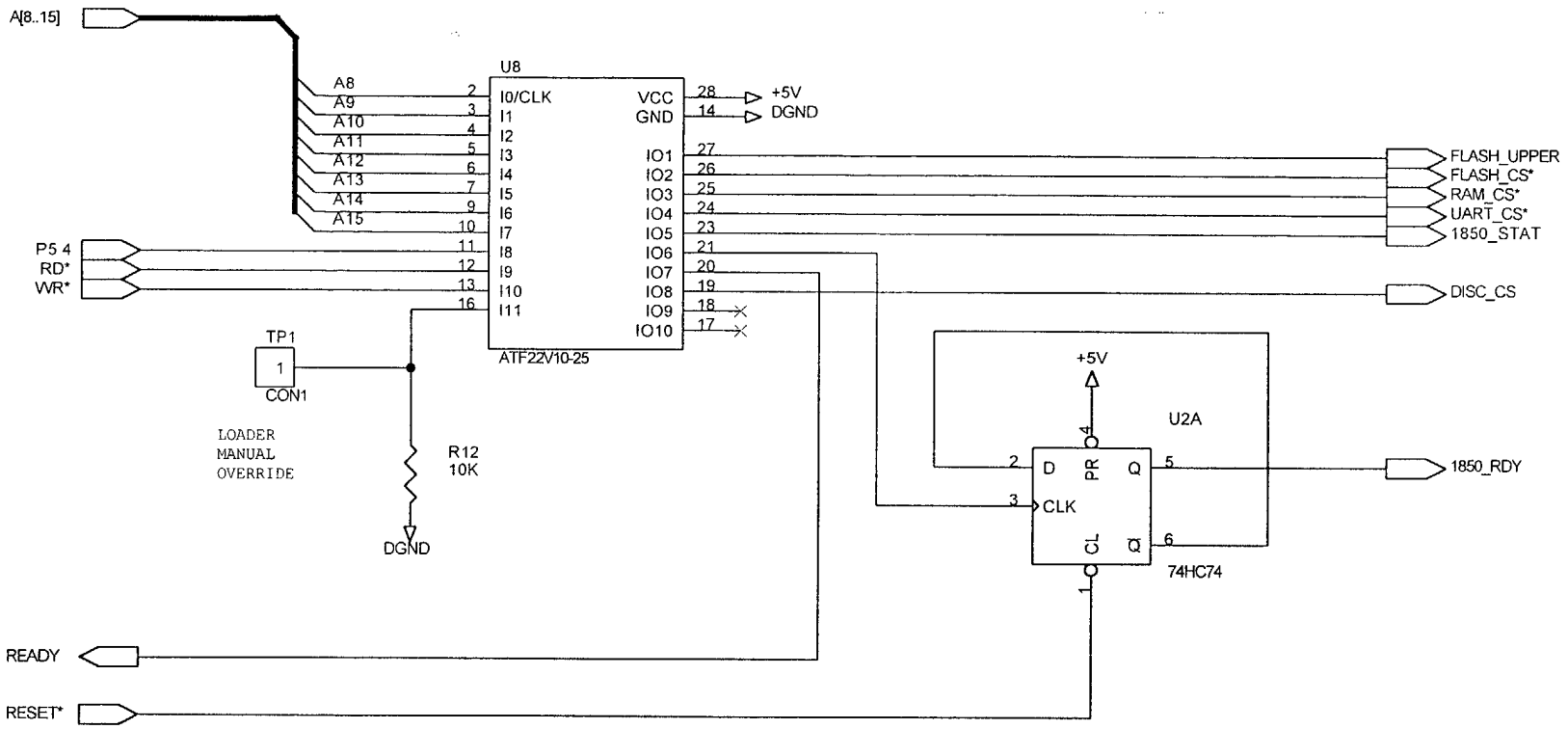



FIG 3


A[8..15]
A8
A9
A10
A11
A12
A13
A14
A15
U8
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
VCC
GND
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
ATF22V10-25
+5V
DGND
FLASH_UPPER
FLASH_CS*
RAM_CS*
UART_CS*
1850_STAT
DISC_CS
P5.4
RD*
WR*
TP1
CON1
LOADER
MANUAL
OVERRIDE
R12
10K
DGND
+5V
U2A
D
PR
Q
CLK
CL
Q
74HC74
1850_RDY
READY
RESET*

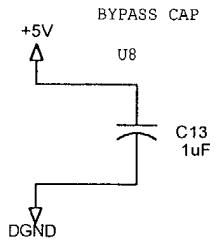

BYPASS CAP
+5V
U8
C13
1uF
DGND

FIG 4

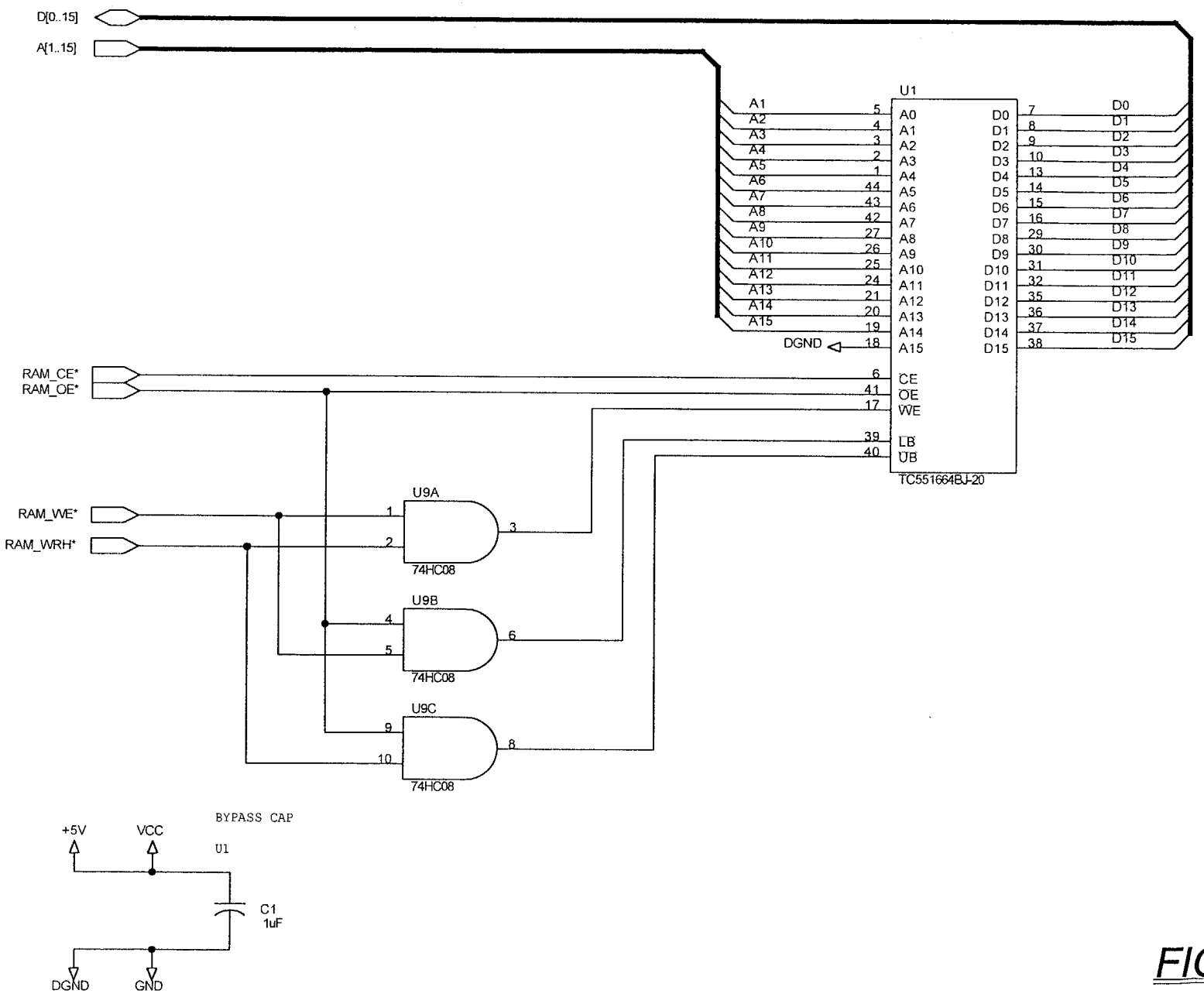
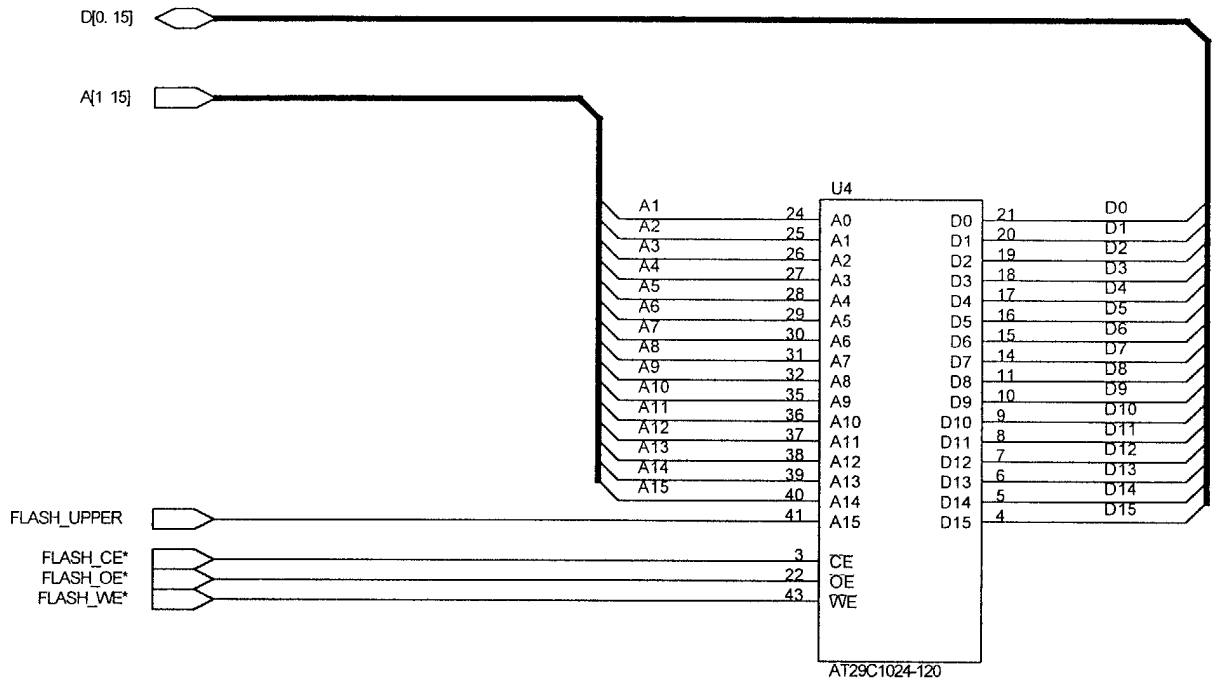

D[0..15]
A[1..15]
U1
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
DGND
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
CE
OE
WE
LB
UB
TC551664BJ-20
RAM_CE*
RAM_OE*
RAM_WE*
RAM_WRH*
U9A
U9B
U9C
74HC08
BYPASS CAP
+5V
VCC
U1
C1
1uF
DGND
GND

FIG 5



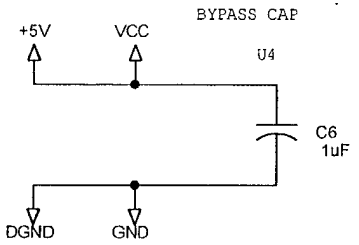
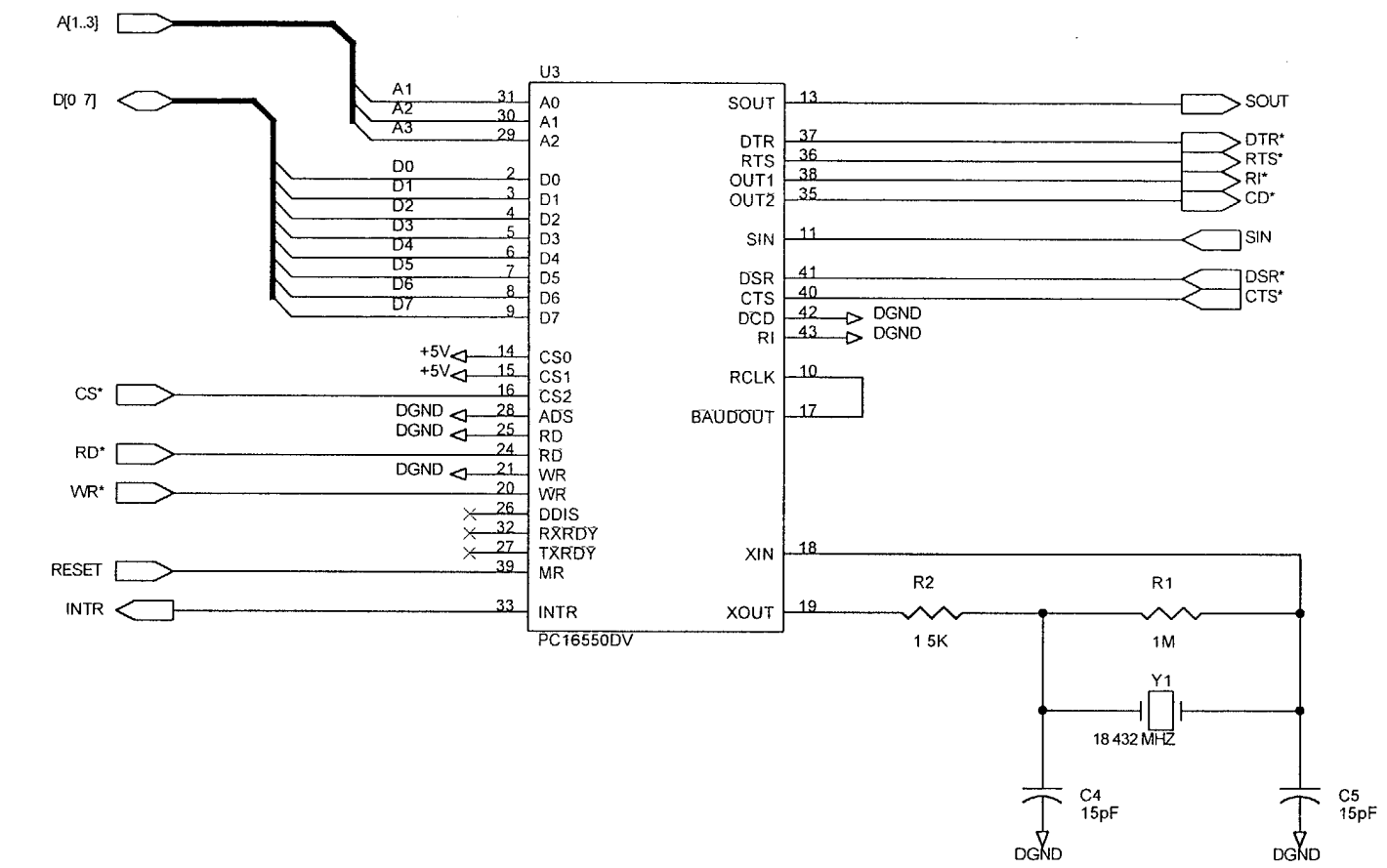




FIG 6



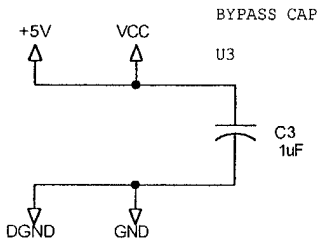
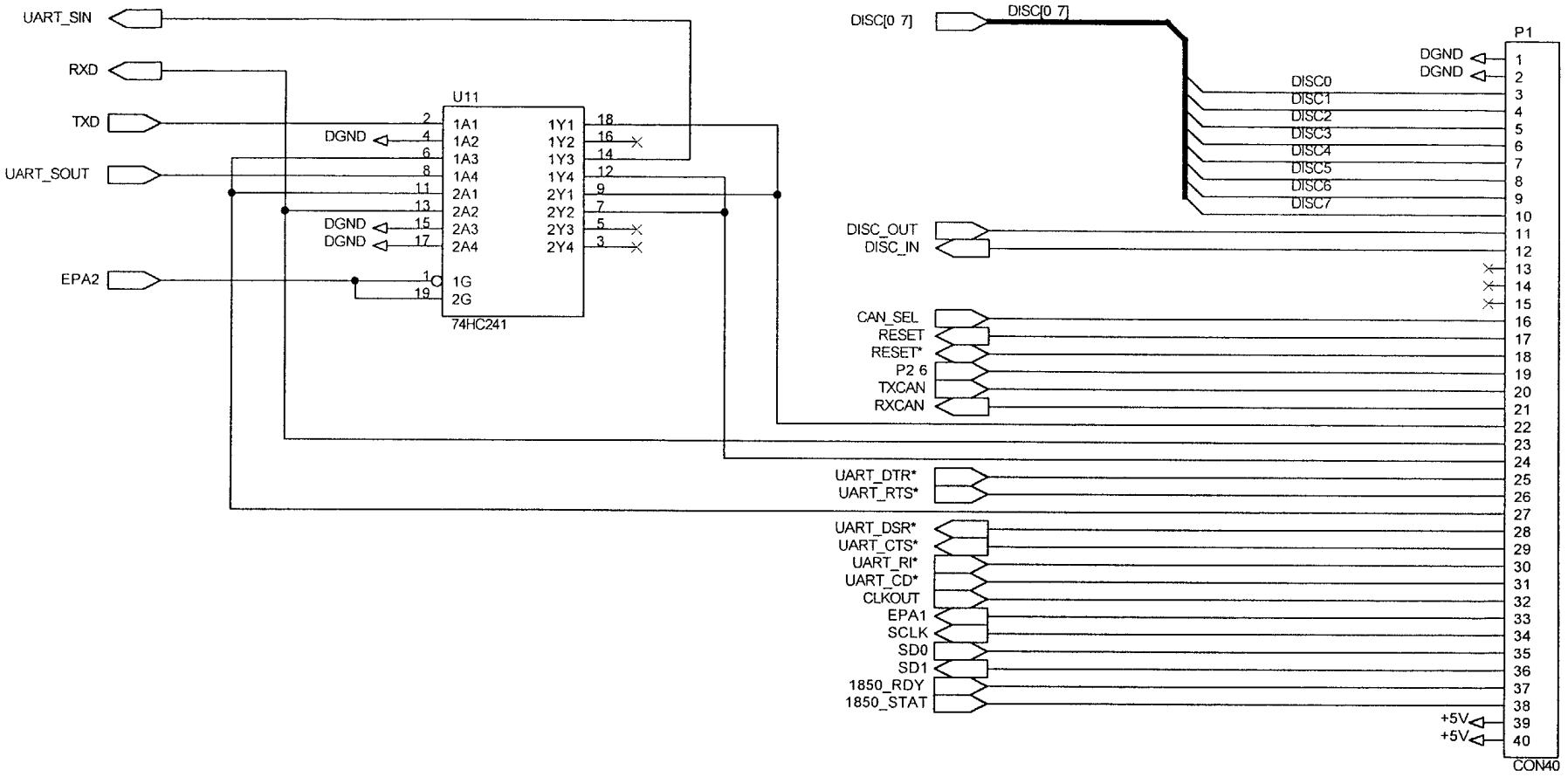




FIG 7



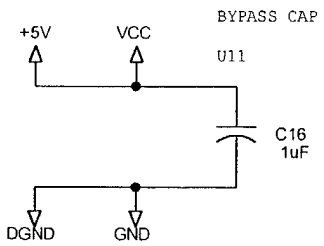
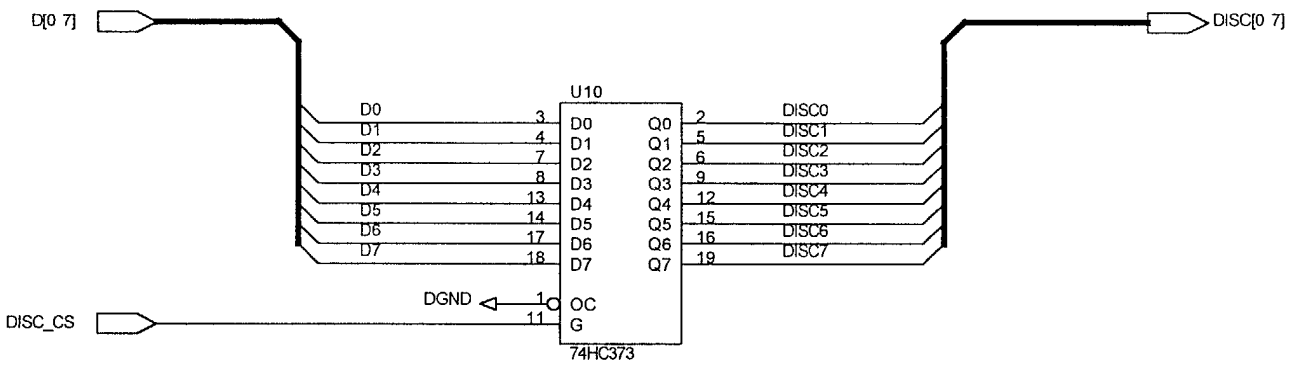




FIG 8



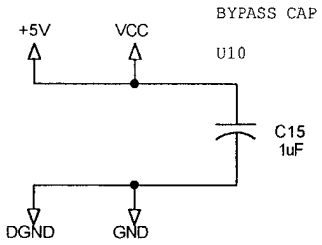
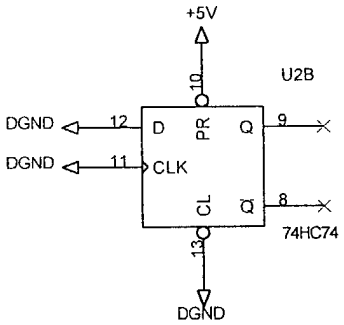
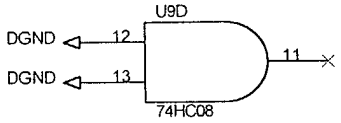




FIG 9



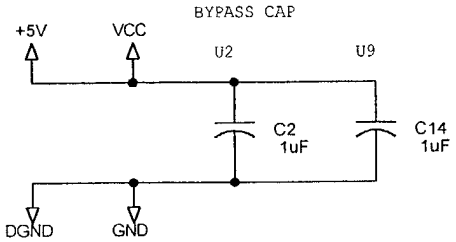




FIG 10

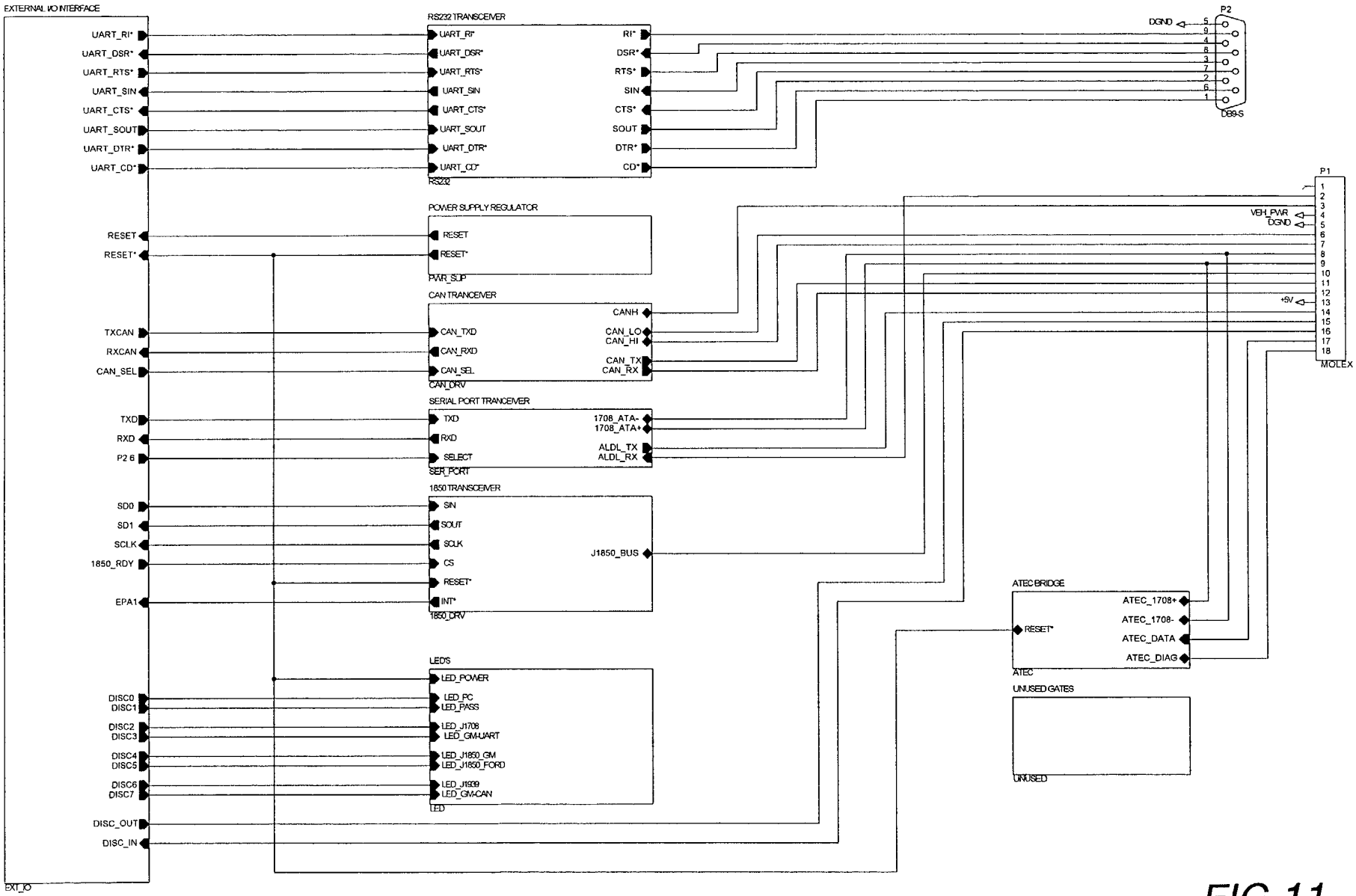

EXTERNAL I/O INTERFACE
UART_RI*
UART_DSR*
UART_RTS*
UART_SIN
UART_CTS*
UART_SOUT
UART_DTR*
UART_CD*
RESET
RESET*
TXCAN
RXCAN
CAN_SEL
TXD
RXD
P2.6
SD0
SD1
SCLK
1850_RDY
EPA1
DISC0
DISC1
DISC2
DISC3
DISC4
DISC5
DISC6
DISC7
DISC_OUT
DISC_IN
EXT_IO
RS232 TRANSCEIVER
UART_RI*
UART_DSR*
UART_RTS*
UART_SIN
UART_CTS*
UART_SOUT
UART_DTR*
UART_CD*
RI*
DSR*
RTS*
SIN
CTS*
SOUT
DTR*
CD*
RS232
POWER SUPPLY REGULATOR
RESET
RESET*
PWR_SUP
CAN TRANCEIVER
CAN_TXD
CAN_RXD
CAN_SEL
CANH
CAN_LO
CAN_HI
CAN_TX
CAN_RX
CAN_DRV
SERIAL PORT TRANCEIVER
TXD
RXD
SELECT
1708_ATA-
1708_ATA+
ALDL_TX
ALDL_RX
SER_PORT
1850 TRANSCEIVER
SIN
SOUT
SCLK
CS
RESET*
INT*
J1850_BUS
1850_DRV
LED'S
LED_POWER
LED_PC
LED_PASS
LED_J1708
LED_GM-UART
LED_J1850_GM
LED_J1850_FORD
LED_J1939
LED_GM-CAN
LED
P2
DGND
D89-S
P1
VEH_PWR
DGND
+5V
MOLEX
ATEC BRIDGE
RESET*
ATEC_1708+
ATEC_1708-
ATEC_DATA
ATEC_DIAG
ATEC
UNUSED GATES
UNUSED

FIG 11

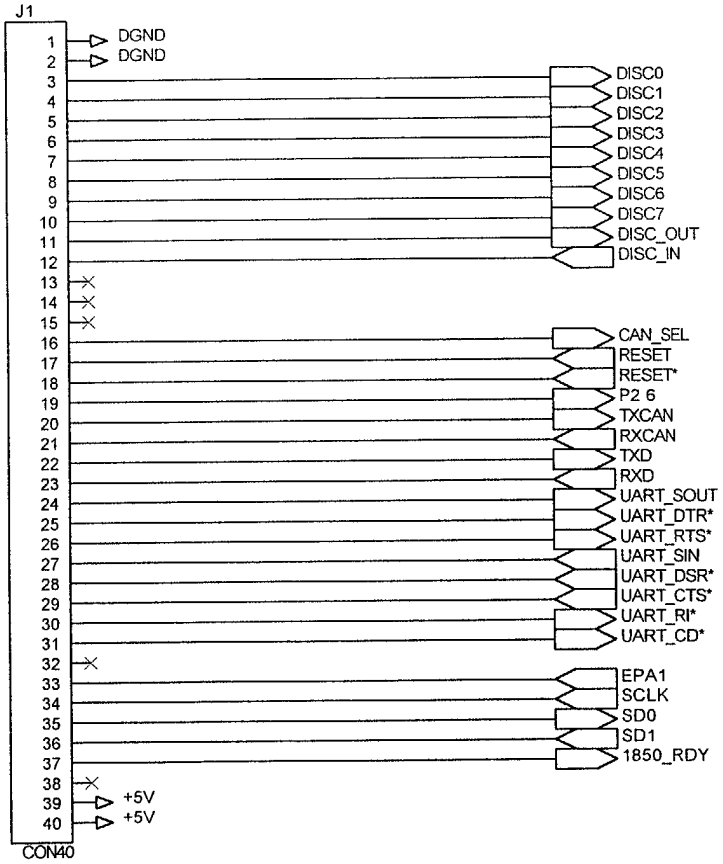
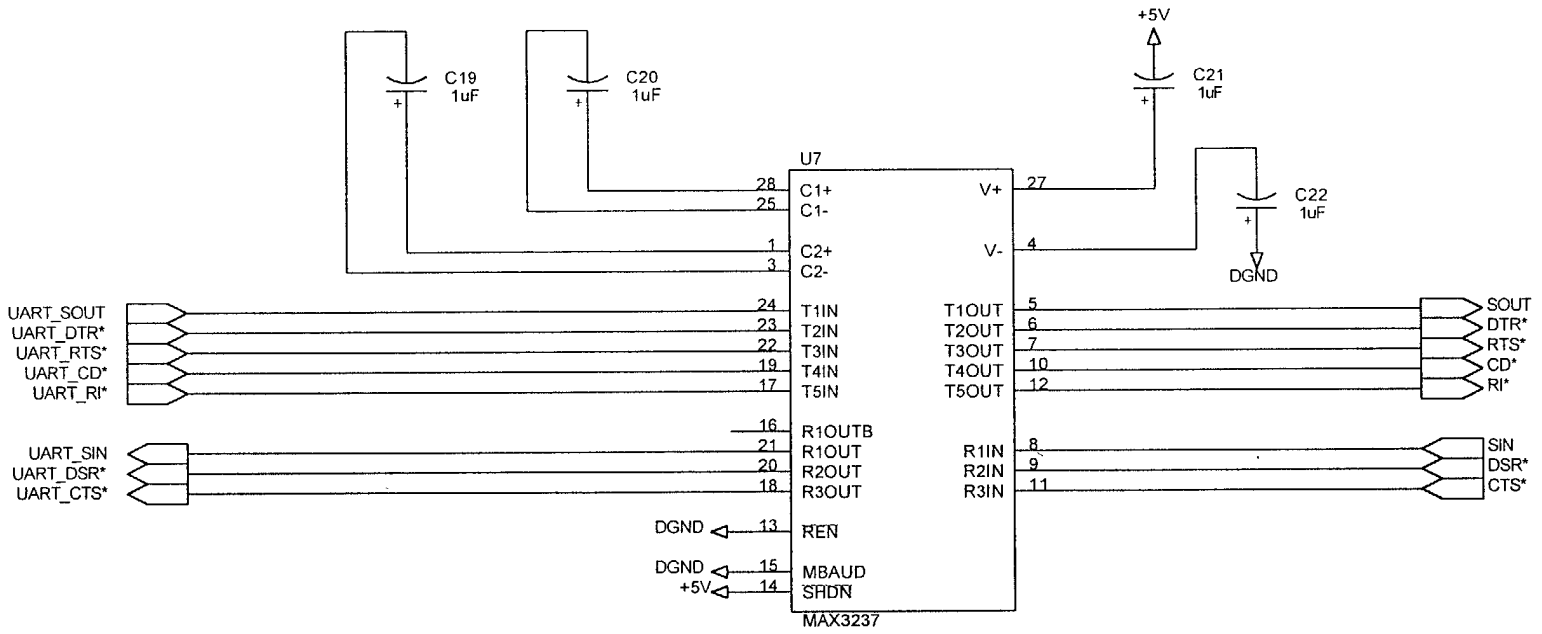

J1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
CON40
DGND
DGND
DISC0
DISC1
DISC2
DISC3
DISC4
DISC5
DISC6
DISC7
DISC_OUT
DISC_IN
CAN_SEL
RESET
RESET*
P2 6
TXCAN
RXCAN
TXD
RXD
UART_SOUT
UART_DTR*
UART_RTS*
UART_SIN
UART_DSR*
UART_CTS*
UART_RI*
UART_CD*
EPA1
SCLK
SD0
SD1
1850_RDY
+5V
+5V

FIG 12


C19
1uF
C20
1uF
+5V
C21
1uF
U7
C1+
C1-
C2+
C2-
V+
V-
C22
1uF
DGND
UART_SOUT
UART_DTR*
UART_RTS*
UART_CD*
UART_RI*
T1IN
T2IN
T3IN
T4IN
T5IN
T1OUT
T2OUT
T3OUT
T4OUT
T5OUT
SOUT
DTR*
RTS*
CD*
RI*
UART_SIN
UART_DSR*
UART_CTS*
R1OUTB
R1OUT
R2OUT
R3OUT
R1IN
R2IN
R3IN
SIN
DSR*
CTS*
DGND
REN
DGND
MBAUD
+5V
SHDN
MAX3237

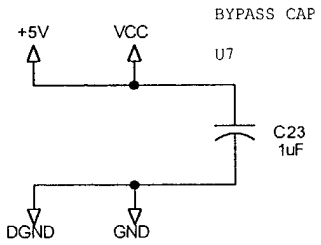
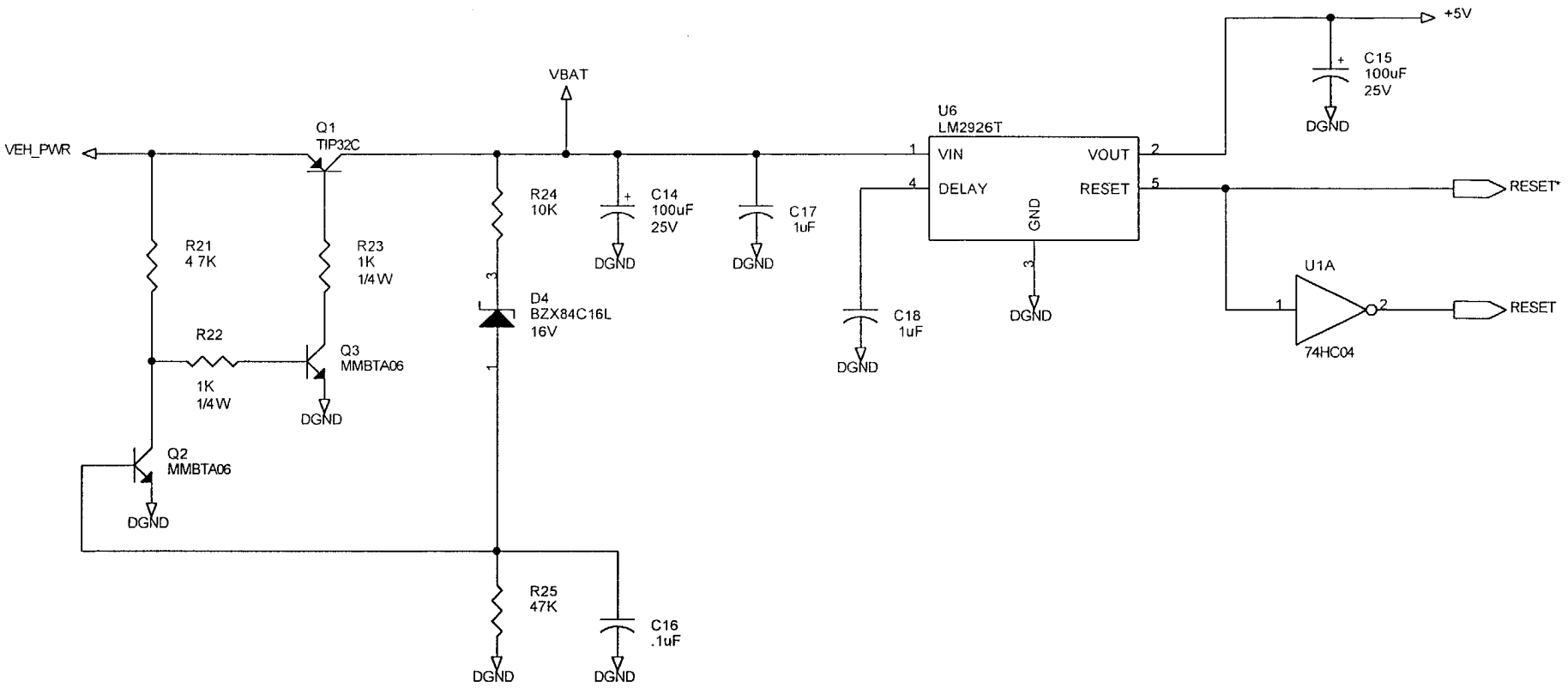

BYPASS CAP
+5V
VCC
U7
C23
1uF
DGND
GND

FIG 13



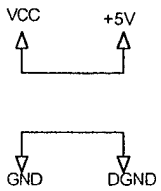




FIG 14

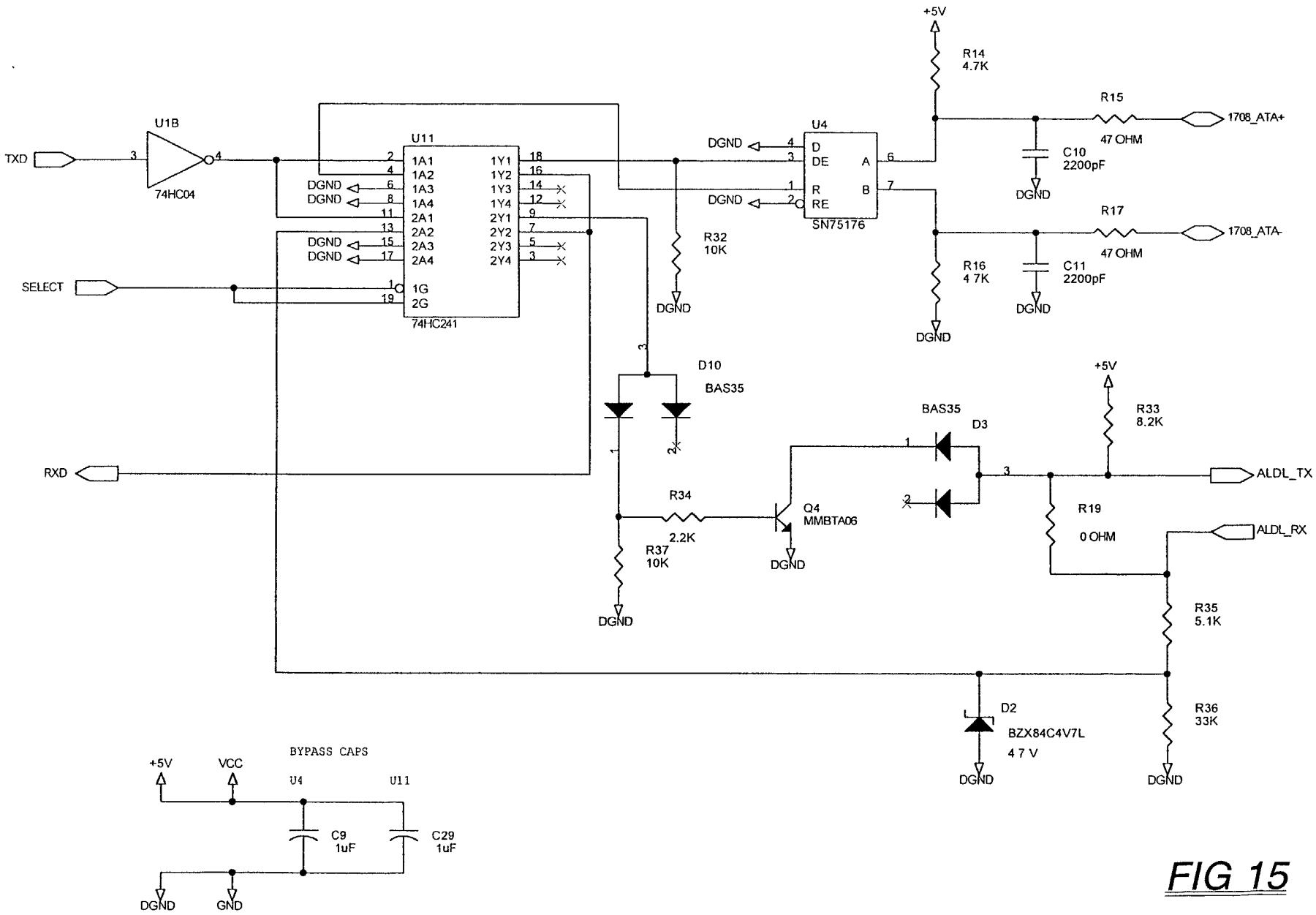
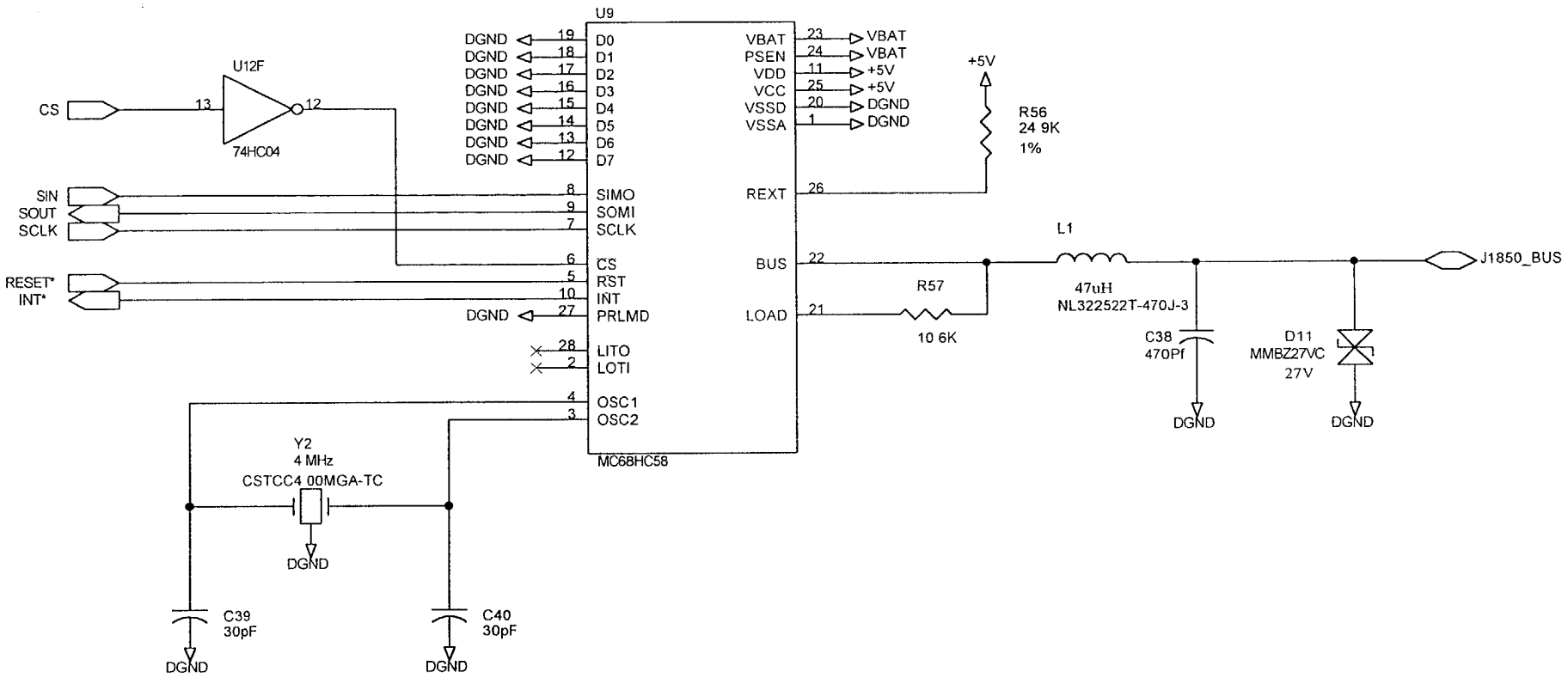

U1B
74HC04
TXD
SELECT
RXD
U11
74HC241
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1G
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
DGND
U4
SN75176
D
DE
R
RE
A
B
+5V
R14
4.7K
R15
47 OHM
1708_ATA+
C10
2200pF
R17
47 OHM
1708_ATA-
C11
2200pF
R16
4 7K
R32
10K
D10
BAS35
BAS35
D3
R33
8.2K
ALDL_TX
R34
2.2K
Q4
MMBTA06
R37
10K
R19
0 OHM
ALDL_RX
R35
5.1K
D2
BZX84C4V7L
4 7 V
R36
33K
BYPASS CAPS
VCC
C9
1uF
C29
1uF
GND

FIG 15




BYPASS
CAPS

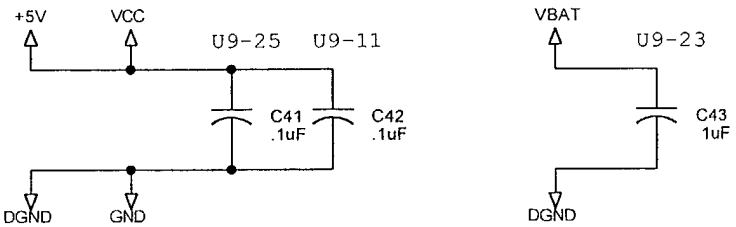
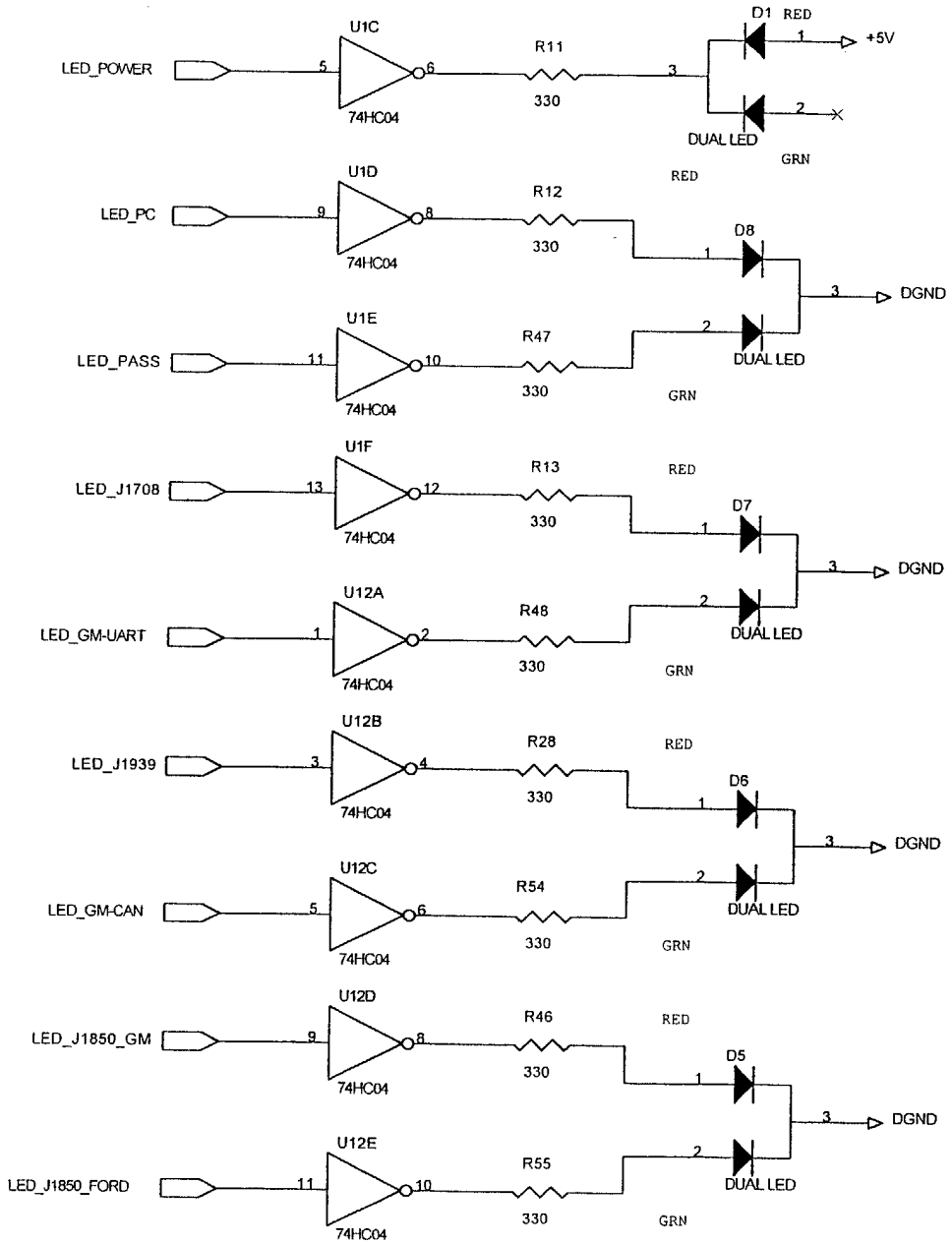



FIG 16



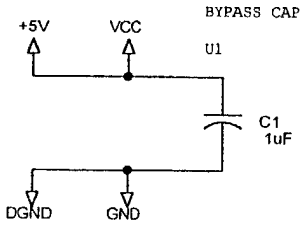




FIG 17

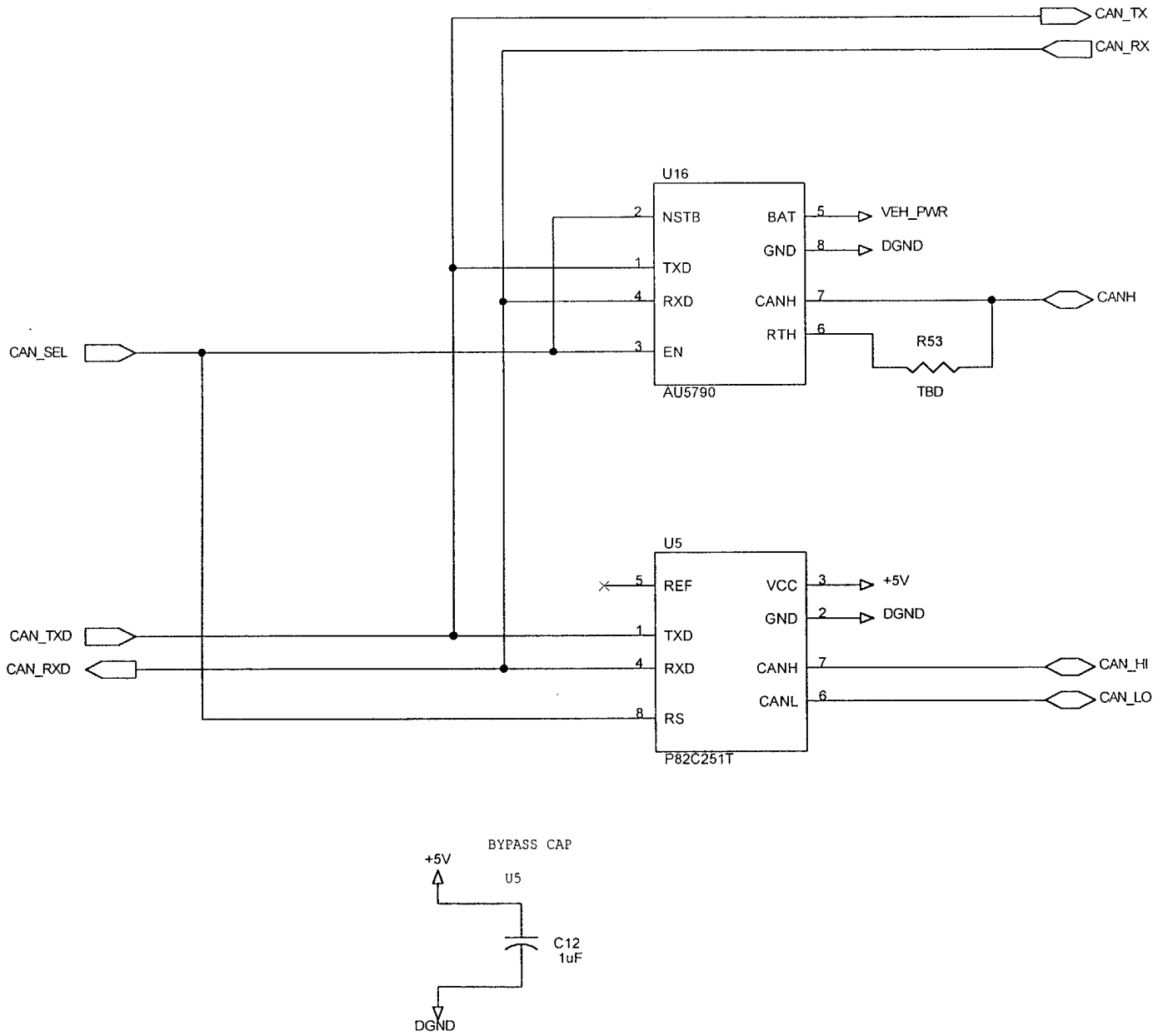



FIG 18

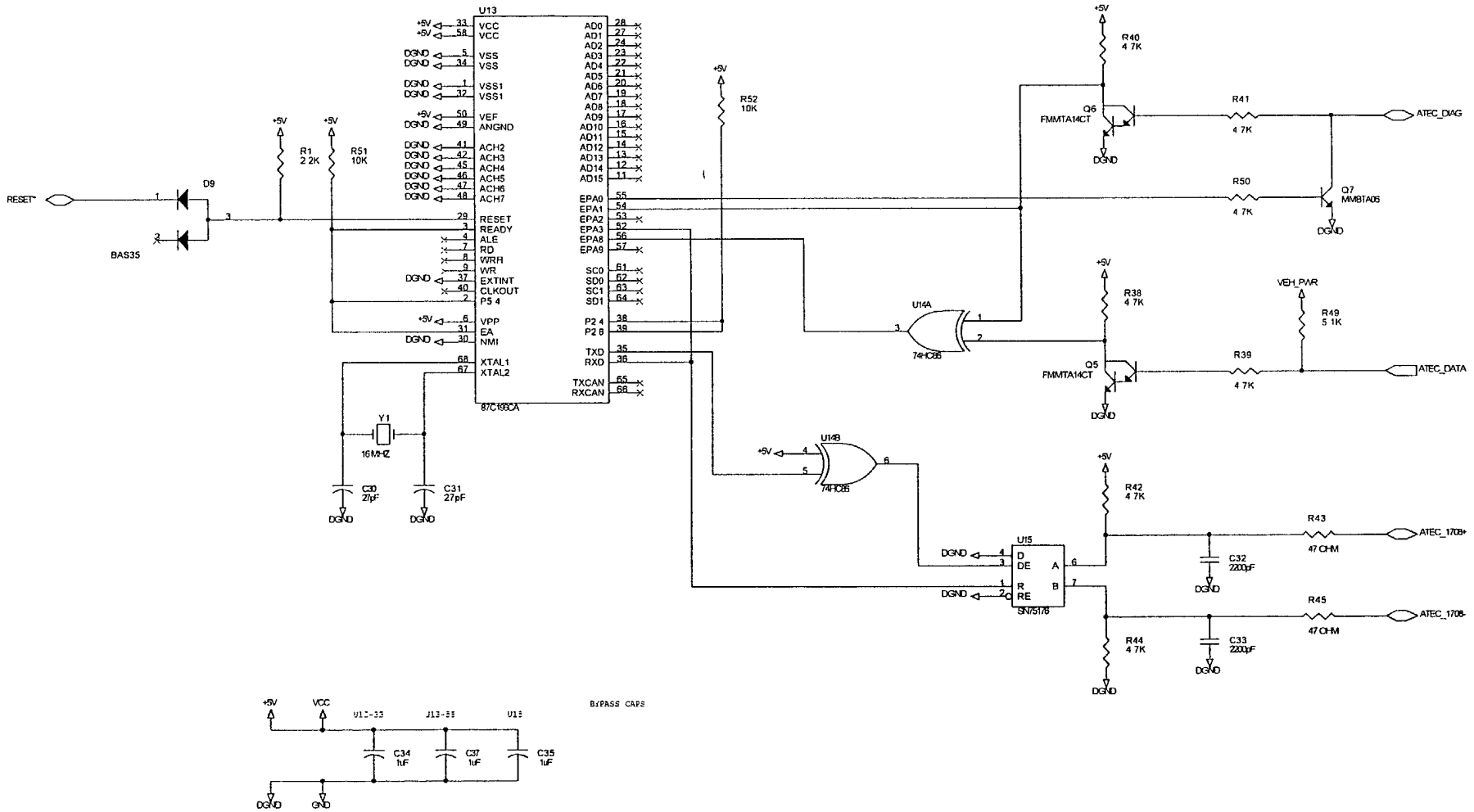
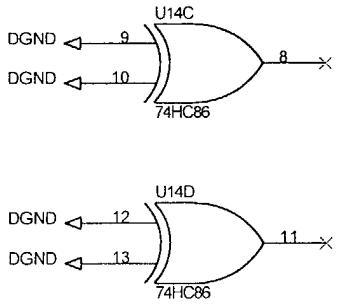

U13
87C196CA
RESET*
BAS35
D9
R1
2.2K
R51
10K
R52
10K
Y1
16MHZ
C30
27pF
C31
27pF
R40
4.7K
Q6
FMMTA14CT
R41
4.7K
ATEC_DIAG
R50
4.7K
Q7
MMBTA06
U14A
74HC86
R38
4.7K
VEH_PWR
R49
5.1K
Q5
FMMTA14CT
R39
4.7K
ATEC_DATA
U14B
74HC86
R42
4.7K
R43
47 OHM
ATEC_1708+
C32
2200pF
U15
SN75176
R45
47 OHM
ATEC_1708-
C33
2200pF
R44
4.7K
BYPASS CAPS
C34
1uF
C37
1uF
C35
1uF
+5V
VCC
DGND
GND

FIG 19



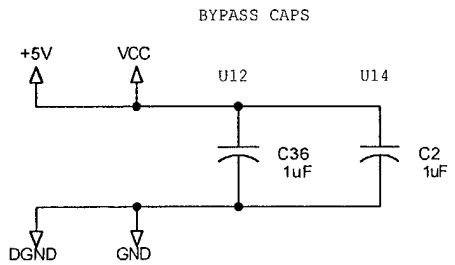




FIG 20

# FIG 21

**LED No. 1 (red)** - Black text, **Power,** indicates power on when illuminated.

# FIG 22

**LED No. 2** - Black text, **Mode,** plus red and green text as shown below:

| Red text | Corresponding meaning for LED when illuminated (red) |
|---|---|
| **DPA** | Normal operation of the DPA unit. Flashes red only when serial communications with PC is occurring. |

| Green text | Corresponding meaning for LED when illuminated (green) |
|---|---|
| **PASS** | Normal DPA operation is suspended, and the protocol pass-through functionality is activated. Indicated by steady flashing green. |

| | |
|---|---|
| **Note:** | Alternating red/green indicates reflash (reprogramming) in progress. |

# FIG 23

**LED No. 3** - Red and green text as shown below:

| Red text | Corresponding meaning for LED when illuminated (red) |
|---|---|
| **J1939** | Dual-wire CAN is in operation: (J1939, Standard CAN or J2284 High-speed CAN) Flashes red when valid bus traffic is present. |

| Green text | Corresponding meaning for LED when illuminated (green) |
|---|---|
| **SW CAN** | Single-wire CAN is in operation: J2411 (if implemented). Flashes green for bus traffic. |

FIG 24

**LED No. 4** - Red and green text as shown below:

| Red text | Corresponding meaning for LED when illuminated (red) |
|---|---|
| **J1850** | Chrysler J1850 protocol is in operation (if implemented). Flashes red for bus traffic. |

| Green text | Corresponding meaning for LED when illuminated (green) |
|---|---|
| **Class II** | GM Class II J1850 protocol is in operation. Flashes green for bus traffic. |

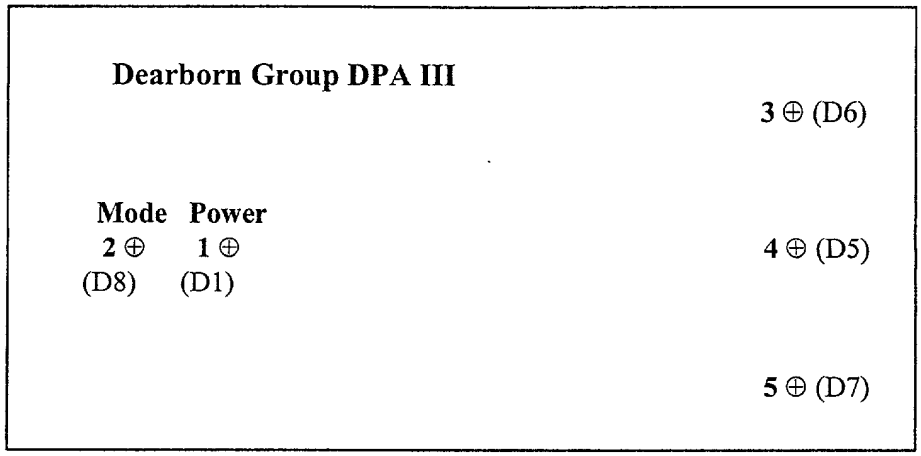
FIG 25

**LED No. 5** - Red and green text as shown below:

| Red text | Corresponding meaning for LED when illuminated (red) |
|---|---|
| **J1708** | J1708 protocol is in operation. Flashes red for bus traffic |

| Green text | Corresponding meaning for LED when illuminated (green) |
|---|---|
| **UART** | One of several UART protocols is in operation: GM Class I (ALDL), ISO 9141-2, ISO 9141-1989, ISO-9141-Special (for Case). Flashes green for bus traffic. |

# FIG 26




**Note:** Characters within parenthesis refer to schematic designations (Fig.17).